

WHAT IS CLAIMED IS:

- 5 *Sub A2* 1. A semiconductor, comprising:
a fractional portion of a semiconductor wafer having a plurality of
integrated circuit chips thereon, such chips being separated by separating
regions in the fractional portion of the wafer;
a plurality of electrical components, each one being associated with, and
adjacent to, a corresponding one of the chips.
- 10 2. The semiconductor recited in claim 1 wherein the electrical components are
voltage generators.
- 15 *Sub A2* 3. The semiconductor recited in claim 2 wherein each one of the components is
disposed in the separating region,
- 20 4. The semiconductor recited in claim 3 wherein the electrical components are
voltage generators
- 25 *Sub A2* 5. The semiconductor recited in claim 1 wherein each one of the voltage
generators has an electrical contact and wherein such package includes:
a dielectric member having an electrical conductor thereon, such electrical
conductor being electrically connected to the plurality of electrical contacts of the
plurality of chips to electrically interconnect such plurality of chips, portions of the
electrical conductor spanning the regions in the fractional portion of the wafer.
- 30 6. A semiconductor, comprising:
a fractional portion of a semiconductor wafer having a plurality of
integrated circuit chips thereon, such chips being separated by separating
regions in the fractional portion of the wafer;
a plurality of sets of electrical components, each set being associated
with, and adjacent to, a corresponding one of the chips; and
an electrical conductor electrically connecting the plurality of electrical
selected one or ones of the electrical components to the chips with portions of the

electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

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- 5 7. The semiconductor recited in claim 6 wherein each set having a plurality of different electrical components.

8. A method for forming a semiconductor, comprising:
providing a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

10 providing a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

15 providing an electrical conductor to electrically connect a selected one or ones of the electrical components to the chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

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9. The method recited in claim 8 wherein each set is provided with a plurality of different electrical components.

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